Journal of Industrial Automation and Electrical Engineering
Vol. 02, No. 01, June 2025, pp. 119~123
ISSN: 3089-1159

Single-phase five level inverter

Nari Amelia Aprilianti Sukma[1], Asnil[1, 2]
[1]Department of Electrical Engineering, Faculty of Engineering, Universitas Negeri Padang, Padang, Indonesia
[2]Centre for Energy and Power Electronics Research (CEPER), Universitas Negeri Padang, Padang, Indonesia

Article Info

Article history:

Received April 02, 2025
Revised May 07, 2025
Accepted May 28, 2025

Keywords:

Single phase inverter
Multilevel inverter
Cascaded H-Bridge
Total Harmonic Distortion
Power electronics
PWM control

ABSTRACT

This paper presents the design and implementation of a single-phase five-level inverter using the Cascaded H-Bridge (CHB) topology. The primary objective of this research is to evaluate the inverter's performance based on the Total Harmonic Distortion (THD) of the output voltage waveform under resistive load conditions. The proposed system consists of two H-Bridge modules powered by independent 23 V DC sources, controlled by an Arduino Mega 2560 and supported by gate driver circuits. The inverter is tested using incandescent lamp as the load. The results show a clearly stepped five-level AC output waveform, characteristic of CHB inverters. THD analysis indicates a distortion level of approximately 12.72%, which is higher than the IEEE 519 standard for sensitive equipment but acceptable for general resistive applications. The results confirm the feasibility of CHB-based inverter construction for practical use, while also highlighting opportunities for further optimization, especially in reducing harmonic content. This work contributes to the field of power electronics by providing a practical foundation for developing low-THD, cost-effective multilevel inverters.

Corresponding Author:

Nari Amelia Aprilianti Sukma
Department of Electrical Engineering, Faculty of Engineering, Universitas Negeri Padang
Kampus UNP Pusat, Jl. Prof. Hamka, Air Tawar, Padang 25131, Indonesia
Email: nariamelia1504@gmail.com

1. INTRODUCTION

Inverter devices play a crucial role in energy conversion systems, particularly in renewable energy applications, uninterruptible power supply (UPS) systems, and electric motor drives. The primary function of an inverter is to convert direct current (DC) voltage into alternating current (AC), which can then be used to power household or industrial loads. Conventional two-level inverters are widely used due to their simple structure and control, but they tend to produce output waveforms with high total harmonic distortion (THD) and exhibit lower efficiency in certain applications [1],[2]. As a solution, multilevel inverter technology has seen rapid development over the past decades. This topology offers the ability to generate smoother and more sinusoidal output waveforms by combining multiple voltage levels. One of the most popular topologies is the Cascaded H-Bridge (CHB), which consists of multiple independent H-Bridge modules with separate DC sources to produce stepped output voltages. This topology provides advantages such as modularity, ease of voltage level expansion, and reduced voltage stress across each power switch [3],[4].

The main issue addressed in this study is how to design and build a single-phase five-level inverter based on the CHB topology that can produce an AC voltage waveform close to sinusoidal with low THD. Evaluating the performance of the constructed device is important to determine the feasibility of the system in practical applications [5]. This study proposes the design and construction of a single-phase five-level inverter using two H-Bridge circuits, each controlled by a PWM signal. Each H-Bridge is supplied with an independent 23 V DC source, and the main power switching component used is the IRFP460 MOSFET. An incandescent lamp is used as the load to directly evaluate the inverter's performance. The main focus of the testing is to analyze the output AC waveform and measure the THD value as an indicator of output quality.

The primary contribution of this research lies in the practical implementation of a multilevel inverter using the CHB topology in physical hardware, rather than simulation alone. With this approach, the study aims to provide a tangible understanding of multilevel inverter performance and serve as a foundation for the development of more efficient and cost-effective power conversion systems in the future [6],[7]..

2. METHOD

This research was conducted by designing and constructing a single-phase five-level inverter based on the Cascaded H-Bridge (CHB) topology, digitally controlled to analyze its Total Harmonic Distortion (THD) performance. The main objective of this study is to determine the THD value of the inverter's output under resistive load conditions using an incandescent lamp. The block diagram illustrating single phase five level inverter is presented in Figure 1.

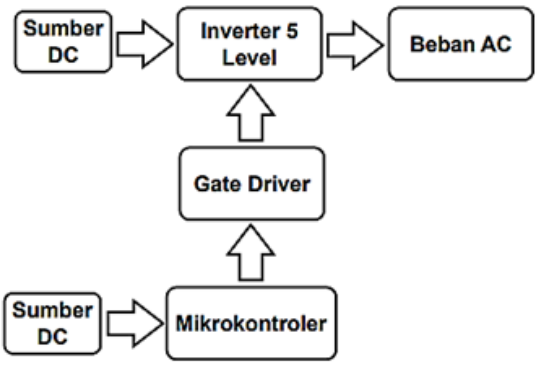


Figure 1. Single phase five level inverter block diagram

The block diagram of the proposed system is shown in Figure 1, which illustrates the main components used in the inverter. The system includes two independent DC sources for the inverter stages, a separate DC supply for the microcontroller, an Arduino Mega 2560 as the control unit, gate driver circuits, a five-level inverter, and an AC load. The CHB topology was selected due to its ability to generate multilevel output voltages that closely approximate a sinusoidal waveform, effectively reducing THD [2],[4],[8]. The system operation procedure is illustrated in the flowchart shown in Figure 2. This flowchart describes the operational stages starting from power supply initialization, PWM signal generation, activation of inverter switching, and data acquisition.

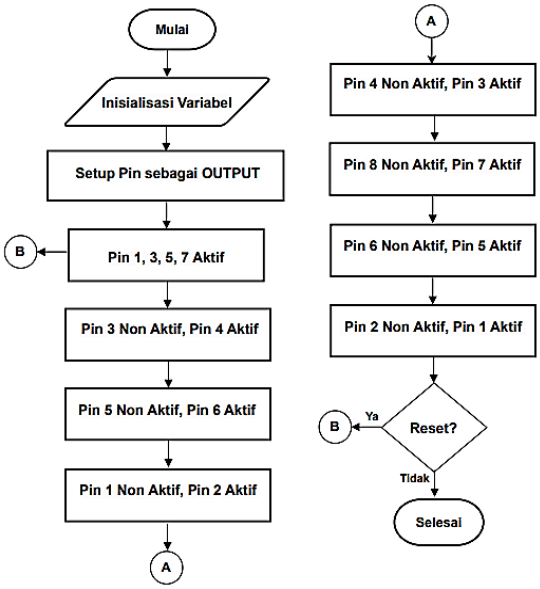


Figure 2. flowchart

The inverter circuit consists of two H-Bridge modules arranged in a cascaded configuration, forming a five-level single-phase output. Each H-Bridge uses four IRFP460 MOSFETs, driven by the same gate driver circuit. Each H-Bridge is powered with a 23V DC supply, enabling the inverter to produce a stepped output voltage with five distinct levels. The detailed inverter circuit design is shown in Figure 3.

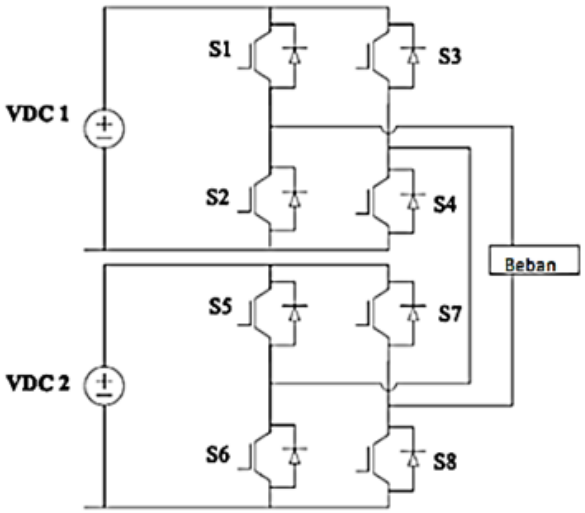


Figure 3. Single-phase five-level inverter circuit

3. RESULTS AND DISCUSSION

This section presents the experimental results and a comprehensive discussion of the performance of the single-phase five-level inverter based on the Cascaded H-Bridge (CHB) topology. The results are shown in the form of waveforms and THD measurements to evaluate inverter performance under resistive load conditions. To document the experimental setup, a photograph of the inverter during testing is presented in Figure 4.

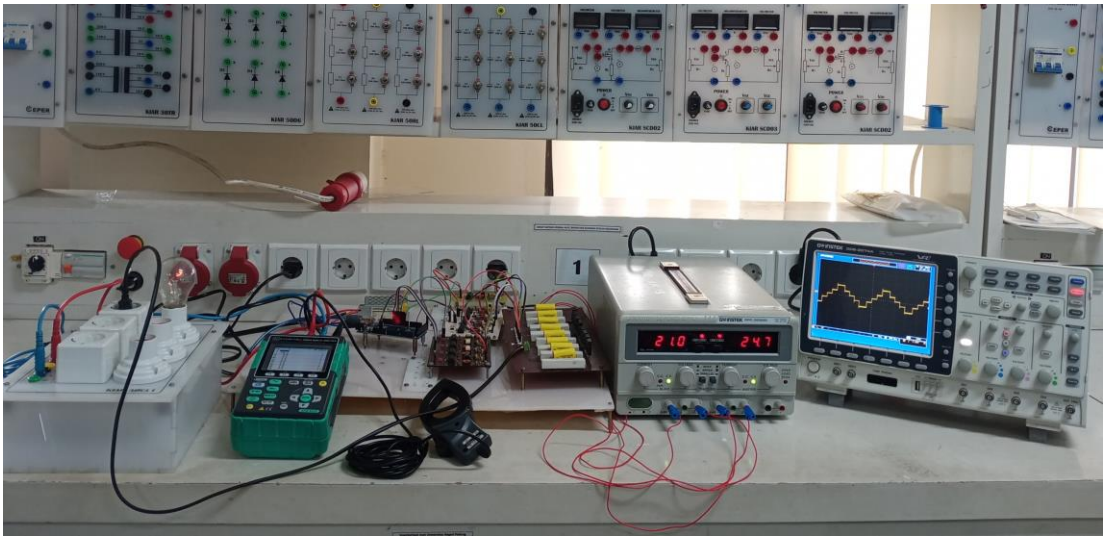


Figure 4. Physical testing of the single-phase five level inverter with incandescent lamp load

3.1 Output Voltage Waveform

The output waveform generated by the inverter under incandescent lamp load is shown in Figure 5. The measured waveform exhibits five distinct voltage levels, as expected from a five-level CHB inverter [4],[9].

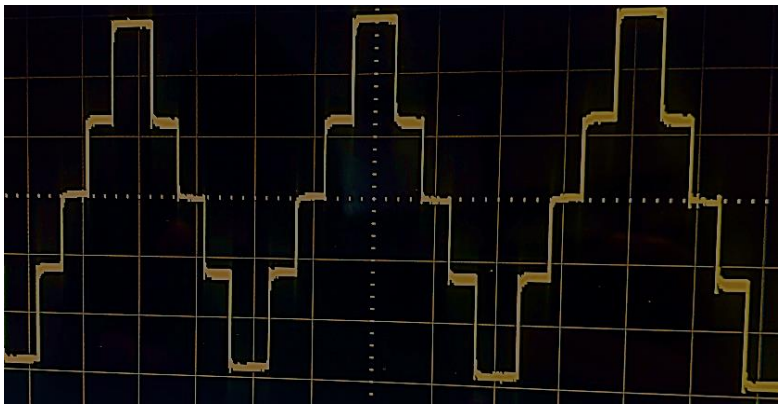


Figure 5. Output voltage waveform of the five-level inverter

The observed voltage levels are : +Vdc (Full positive level), +Vdc/2 (Half positive level), 0V (Neutral point), –Vdc/2 (Half negative level) and –Vdc (Full negative level). These levels confirm that the inverter was able to produce the appropriate stepped AC waveform, validating the correct implementation of PWM signals and switching logic through the Arduino Mega 2560 [7],[10].

3.2 THD Measurement

The Total Harmonic Distortion (THD) of the output waveform was analyzed using the Power Quality Analyzer. The resulting THD value is summarized in Table 1.

Table 1. Measured THD of the five-level inverter output

Parameter	Value
Fundamental frequency	50 Hz
Total harmonic distortion (thd)	12.72%
Load type	Resistive (Incandescent Lamp)
Input dc voltage	2 × 23 V

According to IEEE 519 [14], THD values below 5% are considered suitable for sensitive electrical equipment, while higher values may still be acceptable for general-purpose resistive loads. To support this result, the display of the Power Quality Analyzer used in the THD measurement is shown in Figure 6.

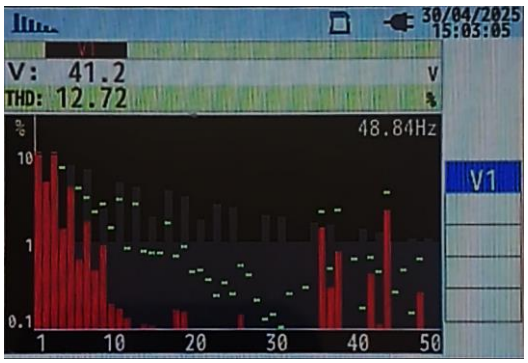


Figure 6. Power Quality Analyzer used for THD measurement displaying waveform and harmonic data

The experiment successfully demonstrated the operation of a five-level single-phase inverter. The output waveform clearly shows the expected stepped structure, a hallmark of multilevel inverter designs [3], [4], [11]. However, the THD value of approximately 12.72% indicates that the waveform still contains significant harmonic content. Several factors likely contribute to the observed harmonic distortion : 1) Limited resolution and switching frequency of the Arduino Mega 2560 [6],[12], 2) Switching delays and dead-time inaccuracies [13], 3) Noise and ripple in the DC power sources, and Suboptimal gate driver performance [7].

While the measured THD exceeds the recommended IEEE threshold for critical loads, the inverter remains functional and suitable for resistive and non-sensitive applications, such as incandescent lamps. For future work, improvements may include : Using a higher-frequency controller (e.g., STM32, FPGA) [15],[16], Applying optimized PWM strategies such as Phase-Shifted PWM or Space Vector PWM [10], [17], and Improving PCB layout and power filtering. The findings confirm that the prototype operates correctly but also indicate room for performance optimization, particularly in reducing THD for broader application suitability.

4. CONCLUSION

This paper has presented the design, implementation, and experimental evaluation of a single-phase five-level inverter based on the Cascaded H-Bridge topology. The system, driven by an Arduino Mega 2560 and gate-driver circuits, successfully produced a stepped AC output consisting of five discrete voltage levels under resistive load. Experimental results demonstrated a clear five-level waveform and a Total Harmonic Distortion (THD) of approximately 12.72%. While this THD exceeds the IEEE 519 recommendation for sensitive equipment, the prototype remains viable for non-critical resistive loads such as incandescent lamps. The measured performance confirms the functionality of the CHB approach but also highlights the need for further optimization to meet stricter harmonic standards.Future work will focus on reducing THD through higher-resolution PWM strategies (e.g., phase-shifted or space-vector PWM), adoption of faster control platforms (such as STM32 microcontrollers or FPGAs), and refinement of power-stage layout and filtering. These improvements are expected to enhance the waveform quality and broaden the inverter's applicability to more demanding electrical loads.

REFERENCES

[1] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron*., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[2] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron*., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] L. G. Franquelo et al., "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag*., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[4] B. Wu, *High-Power Converters and AC Drives*. John Wiley & Sons, 2006.

[5] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl*., vol. 37, no. 2, pp. 611–618, Mar./Apr. 2001.

[6] M. R. Banaei and E. Salary, "A new family of multilevel inverters with the capability of reducing the number of power switches," *European Transactions on Electrical Power*, vol. 21, no. 1, pp. 344–357, Jan. 2011.

[7] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron*., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[8] S. Khomfoi and L. M. Tolbert, "*Multilevel power converters," Power Electronics Handbook*, 2nd ed., Elsevier, 2007.

[9] N. A. Rahim, J. Selvaraj, and C. J. Gajanayake, "Cascaded multilevel inverter with single DC source," in *Proc. IEEE Power Electron. Spec. Conf*., 2007, pp. 256–260.

[10] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE Press, 2003.

[11] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron*., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[12] V. G. Agelidis, A. Balouktsis, and C. Cossar, "Multiple sets of solutions for harmonic elimination PWM bipolar waveforms: Analysis and experimental verification," *IEEE Trans. Power Electron*., vol. 21, no. 2, pp. 415–421, Mar. 2006.

[13] S. Jose and S. P. R. Daniel, "Design and implementation of a multilevel inverter for renewable energy sources," in *Proc. Int. Conf. Renewable Energy Res. Appl*., 2013, pp. 1026–1031.

[14] IEEE Std 519-2014, "*IEEE recommended practice and requirements for harmonic control in electric power systems*," 2014.

[15] T. Mishra and V. Pandey, "THD analysis of cascaded multilevel inverter," *Int. J. Eng. Res. Appl*., vol. 5, no. 4, pp. 51–56, Apr. 2015.

[16] M. K. Mishra, "Control techniques for power quality improvement in renewable energy systems," *Renewable and Sustainable Energy Reviews*, vol. 16, no. 8, pp. 4957–4964, 2012.

[17] H. Patel and V. Agarwal, "PWM techniques for voltage source multilevel inverters: A review," *IEEE Trans. Ind. Electron*., vol. 54, no. 5, pp. 2697–2708, Oct. 2007.

.